

# FQN1N60C

## 600V N-Channel MOSFET

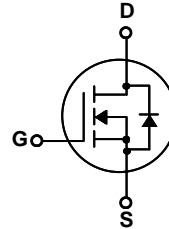
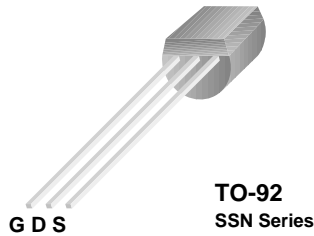
### Features

- 0.3 A, 600 V,  $R_{DS(on)} = 11.5 \Omega @ V_{GS} = 10 \text{ V}$
- Low gate charge ( typical 4.8 nC )
- Low  $C_{rss}$  ( typical 3.5 pF)
- Fast switching
- 100 % avalanche tested
- Improved dv/dt capability

### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.



### Absolute Maximum Ratings

Symbol	Parameter	FQN1N60C	Units
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	0.3
		- Continuous ( $T_C = 100^\circ\text{C}$ )	0.18
$I_{DM}$	Drain Current - Pulsed (Note 1)	1.2	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	33	mJ
$I_{AR}$	Avalanche Current (Note 1)	0.3	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	0.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ )	1	W
	Power Dissipation ( $T_L = 25^\circ\text{C}$ )	3	W
	- Derate above $25^\circ\text{C}$	0.02	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead (Note 6a)	--	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 6b)	--	140	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
1N60C	FQN1N60C	TO-92	--	--	2000ea

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

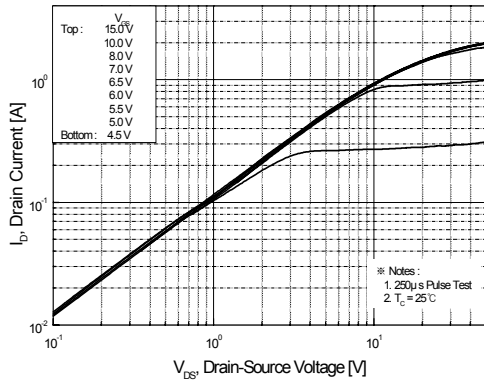
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	600	--	--	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.6	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	--	--	50	μA
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C	--	--	250	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.15 A	--	9.3	11.5	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 0.3 A (Note 4)	--	0.75	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	130	170	pF
C <sub>oss</sub>	Output Capacitance		--	19	25	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	3.5	6	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 1.1 A, R <sub>G</sub> = 25 Ω (Note 4, 5)	--	7	24	ns
t <sub>r</sub>	Turn-On Rise Time		--	21	52	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	13	36	ns
t <sub>f</sub>	Turn-Off Fall Time		--	27	64	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 1.1 A, V <sub>GS</sub> = 10 V (Note 4, 5)	--	4.8	6.2	nC
Q <sub>gs</sub>	Gate-Source Charge		--	0.7	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	2.7	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	0.3	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	1.2	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.3 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.1 A, dI <sub>F</sub> / dt = 100 A/μs (Note 4)	--	190	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.53	--	μC

### Notes:

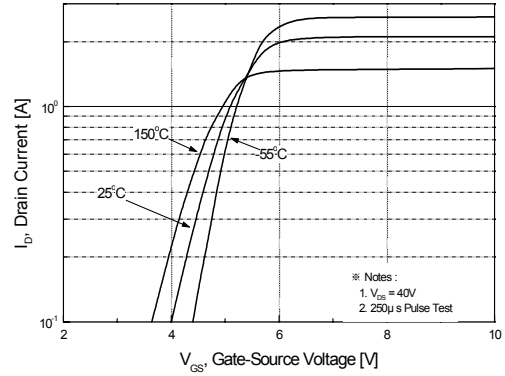
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 59mH, I<sub>AS</sub> = 1.1A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 0.3A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature
6. a) Reference point of the R<sub>θJL</sub> is the drain lead  
 b) When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment  
 (R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance. R<sub>θCA</sub> is determined by the user's board design)

## Typical Performance Characteristics

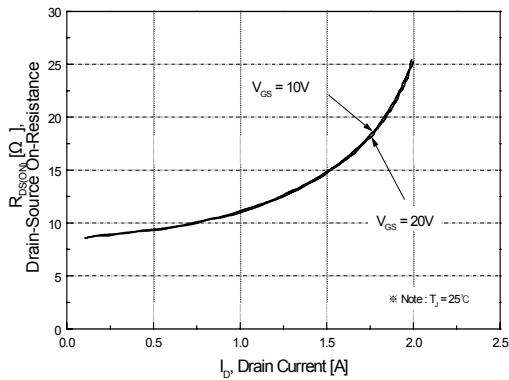
**Figure 1. On-Region Characteristics**



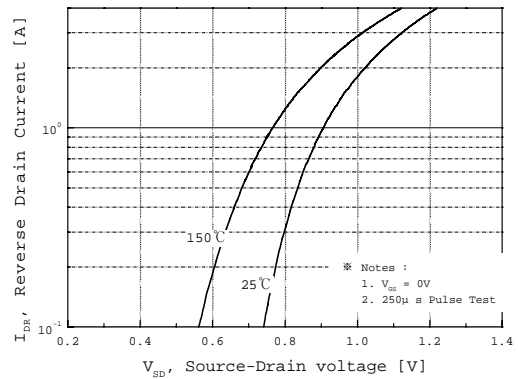
**Figure 2. Transfer Characteristics**



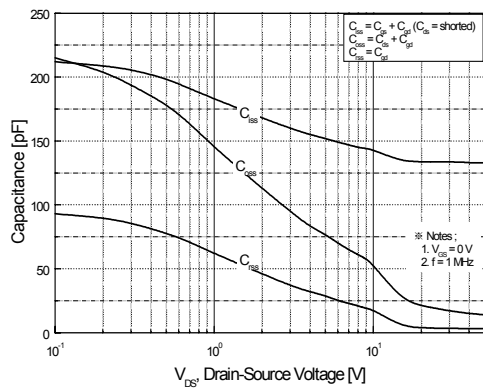
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



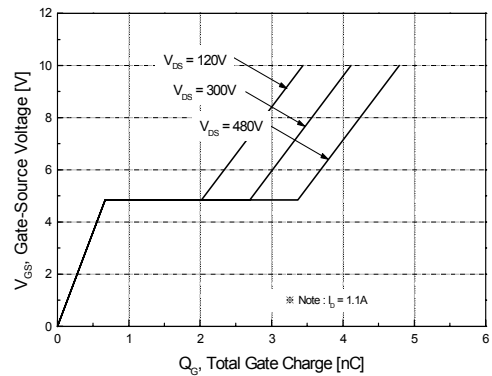
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

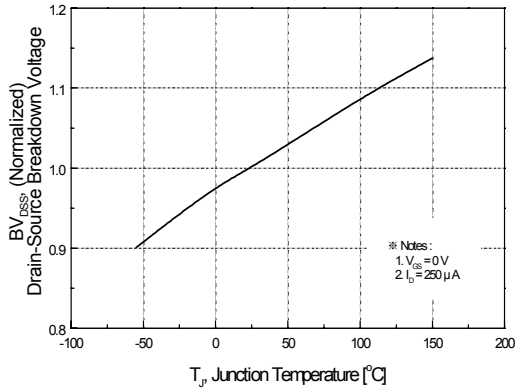


**Figure 6. Gate Charge Characteristics**

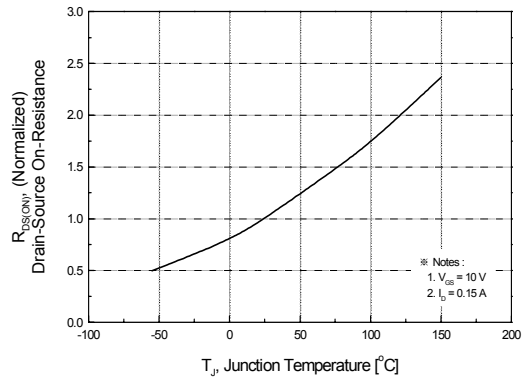


**Typical Performance Characteristics** (Continued)

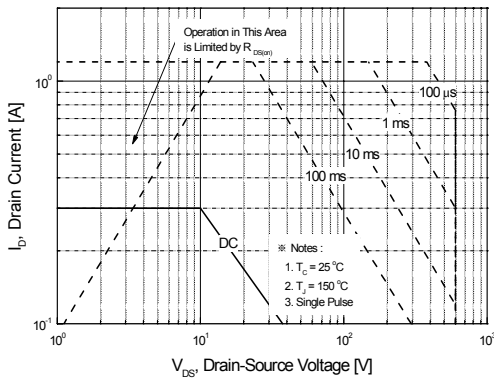
**Figure 7. Breakdown Voltage Variation vs. Temperature**



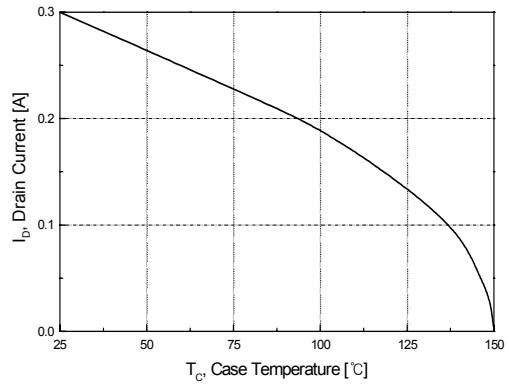
**Figure 8. On-Resistance Variation vs. Temperature**



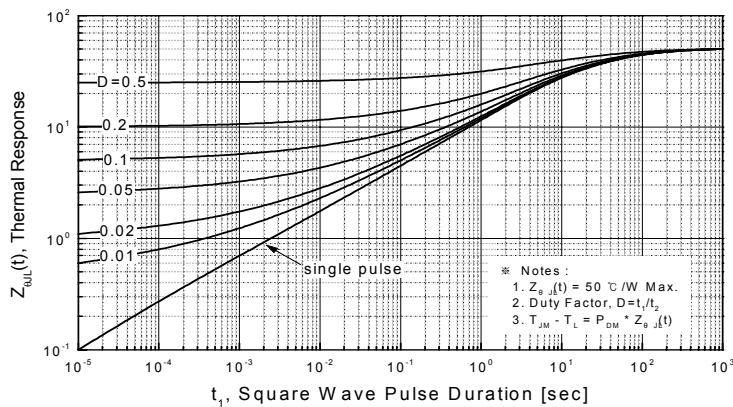
**Figure 9. Maximum Safe Operating Area**



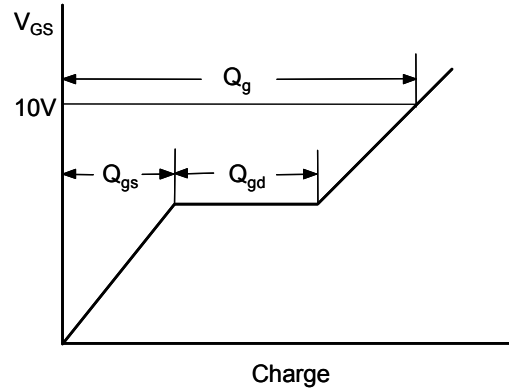
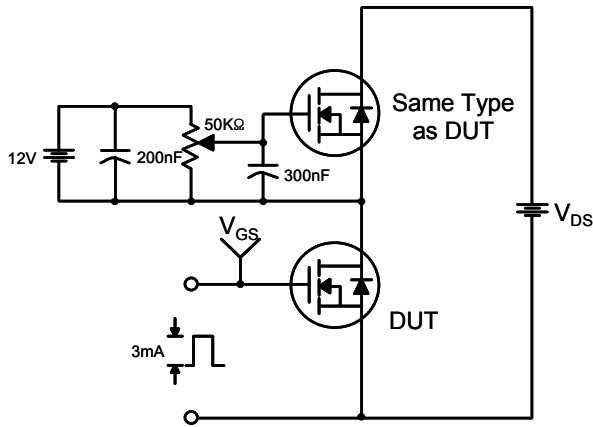
**Figure 10. Maximum Drain Current vs. Case Temperature**



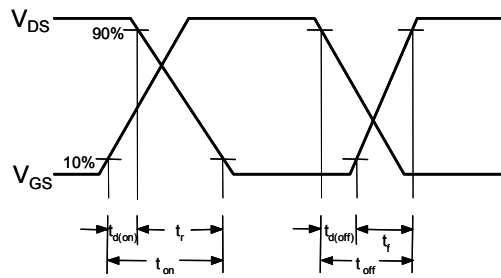
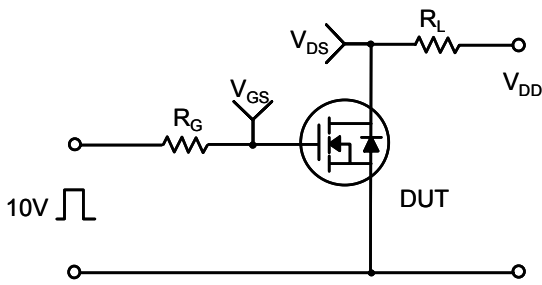
**Figure 11. Transient Thermal Response Curve**



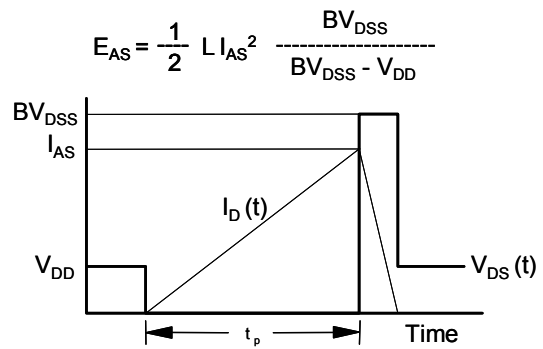
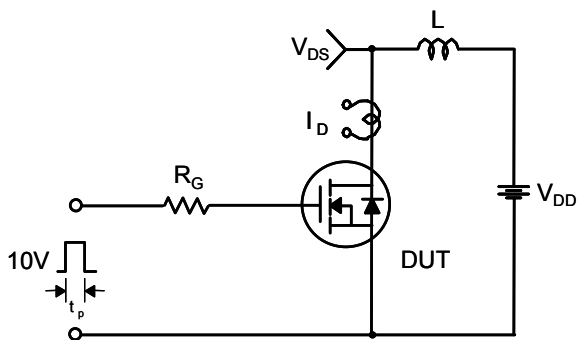
**Gate Charge Test Circuit & Waveform**



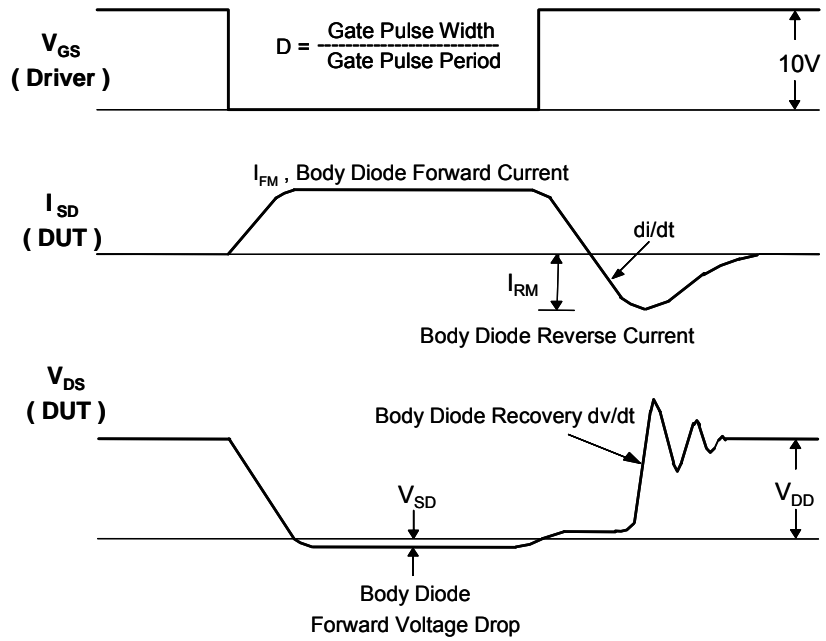
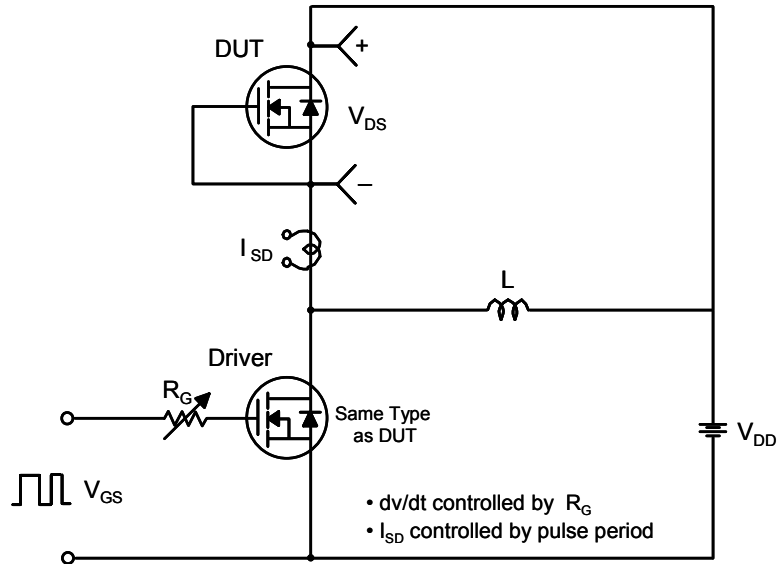
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

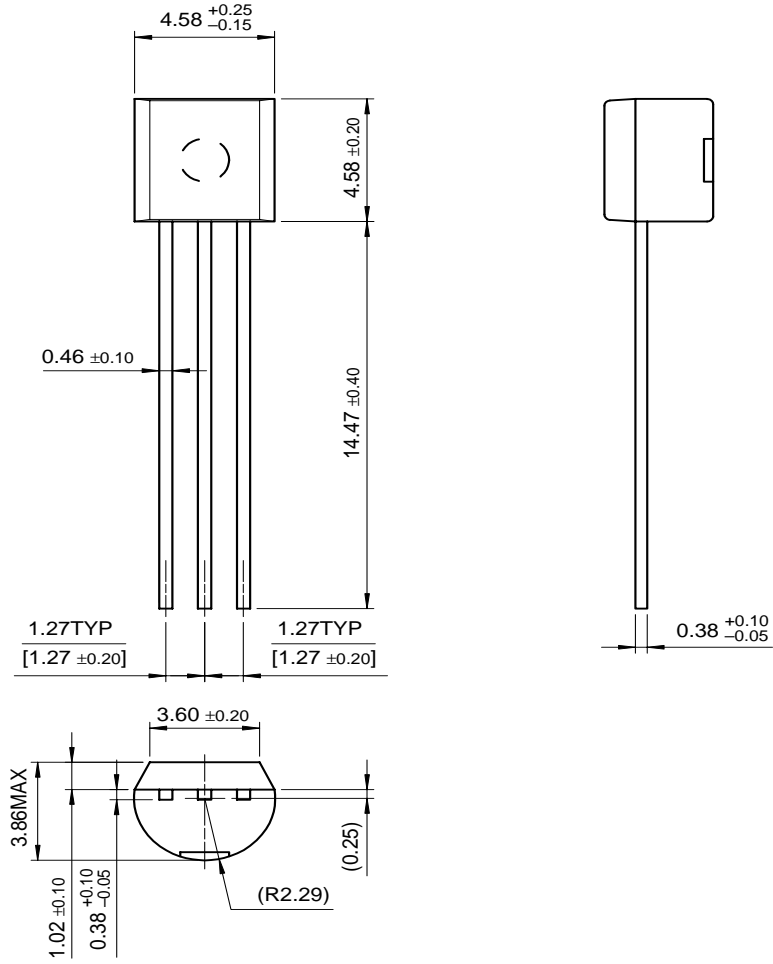


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-92



Dimensions in Millimeters

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